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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,449	06/01/2001	Michael Catherwood	18153.0035	8451

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EXAMINER	
MYERS, PAUL R	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 09/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/870,449	CATHERWOOD ET AL.	
	Examiner	Art Unit	
	Paul R. Myers	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2004*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 6/16/04 have been fully considered but they are not persuasive.

In regards to applicants argument that Yasuda does not teach loading a second instruction within the interrupt service routine into the program counter. This is incorrect. See figures 6A and 6B and Column 4 line 57 to Column 5 line 4.

In regards to applicants argument that Yasuda PN 5,611,061; Zaiki PN 6,292,866 and Laurenti PN 6,658,578 do not teach the claimed fast interrupt. The examiner agrees that Yasuda and Zaiki merely teach decoding the interrupt and as such do not describe a fast interrupt. Thus the 102 rejections to Yasuda and Zaiki are removed. The examiner also notes the claim language does not indicate what a fast interrupt is. The term fast interrupt is so broad as to be interpreted as an interrupt that has a higher priority thus is serviced first, or an interrupt that comes from a device that is a fast device, or an interrupt that is not delayed, or an interrupt that is processed at a higher rate. Laurenti teaches interrupts with higher priority (Column 106 lines 36-47), interrupts from a fast device, and "undelayed" interrupts (Column 117 lines 62-65, Column 110 lines 23-27 and Column 113 lines 54-61) . Thus Laurenti teaches fast interrupts.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Laurenti et al. (USPN 6,658,578; Laurenti).

As per claim 1, Laurenti discloses the claimed invention including a method for processing a low-overhead interrupt, comprising: detecting the occurrence of an interrupt condition that requires servicing (interrupt acknowledging; col. 123-124); determining that the interrupt condition corresponds to a fast interrupt (decodes; fast devices; col. 152); loading a first instruction of an interrupt service routine (ISR) into an instruction register for immediate execution (col. 124, lines 37+; col. 125, lines 17-18); loading an address of a second instruction within the ISR into a program counter (col. 262); and fetching the second ISR instruction while executing the first ISR instruction (prefetch; col. 11, lines 44 et seq. ; Table 1; parallelism; see also col. 124, lines 65 et seq.; col. 125, lines 3 et seq.).

As per claim 2, Laurenti discloses the method according to claim 1, further comprising: storing contents of a prefetch register into a holding register based on the determining (e.g. IFGxx flag register; col. 123, lines 37-42).

As per claim 3, Laurenti discloses the method according to claim 1, further comprising: storing a program counter value and a status register value onto a stack based on the determining (e.g. col. 125, lines 26-38).

As per claim 4, Laurenti discloses the method according to claim 3, further comprising: executing remaining instructions in the ISR; and returning from the ISR (col. 263).

As per claim 5, Laurenti discloses the method according to claim 4, wherein the returning comprises: restoring an instruction from the holding register into the prefetch register (col. 125, lines 22-30; col. 263).

As per claim 6, Laurenti discloses the method according to claim 5, wherein the returning further comprises popping a program counter value and a status register value from a stack and storing them into respective program counter and status registers (col. 125, lines 22-30; col. 263).

As per claim 7, Laurenti discloses the method according to claim 6, further comprising executing the instruction restored to the prefetch register and fetching the next instruction for execution based on the status register and the program counter register (col. 125, lines 22-38; col. 263).

As per claim 8, Laurenti discloses the method according to claim 7, wherein the status register after the returning from the ISR indicates that a repeat instruction is being processed and

wherein a loop counter is decremented after executing the instruction restored to the prefetch register (repeat, loops and nested loops are supported in the Laurenti system; see col. 263, lines 1 et seq.; col. 265).

As per claim 9, Laurenti discloses a processor (100) for handling low-overhead interrupts, comprising: a first interrupt instruction register (106) storing the first interrupt instruction of a plurality of interrupt service routines; a holding register (e.g. IFGxx flag register; col. 123, lines 37-42); an interrupt vector register (col. 8, lines 64-65; col. 123, lines 52-60); a program counter (e.g. PC register; or 532, 536, 530, 534; col. 10, lines 5-20; col. 125, line 3); and interrupt logic coupled to the registers, upon an interrupt, the interrupt logic a) loading a first instruction of an interrupt service routine (ISR) from the first interrupt instruction register into an instruction register for immediate execution (col. 124, lines 37+; col. 125, lines 17-18) and b) loading an address of a second instruction within the ISR into the program counter based on the interrupt vector register and executing the ISR (prefetch; col. 11, lines 44 et seq. ; Table 1; parallelism; see also col. 124, lines 65 et seq.; col. 125, lines 3 et seq.).

As per claim 10, Laurenti discloses the processor according to claim 9, wherein the interrupt logic further c) stores the next instruction for regular execution upon return from the interrupt into a holding register (prefetch; col. 125, lines 26-30).

As per claim 11, Laurenti discloses the processor according to claim 9, wherein the interrupt logic further stores a program counter value and a status register value onto a stack (e.g. col. 125, lines 33-38).

As per claim 12, Laurenti discloses the processor according to claim 11, wherein the interrupt logic causes a return from the ISR at the end of the ISR (col. 125, lines 22-30).

As per claim 13, Laurenti discloses the processor according to claim 12, wherein upon the return, the interrupt logic restores an instruction from the holding register into a register for execution (col. 125, lines 22-30).

As per claim 14, Laurenti discloses the processor according to claim 13, wherein upon the return the interrupt logic further pops a program counter value and a status register value from a stack and stores them respectively into the program counter and a status registers (col. 125, lines 22-38; col. 263).

As per claim 15, Laurenti discloses the processor according to claim 14, wherein the status register after the returning from the ISR indicates that a repeat instruction is being processed and wherein a loop counter is decremented after executing the instruction restored to the register (repeat, loops and nested loops are supported in the Laurenti system; see col. 263, lines 1 et seq.; col. 265).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

PN 4,709,324 to Kloker teaches handling interrupts with prefetching.

PN 5,623,646 to Clarke teaches recognizing and handling fast and regular interrupts differently.

PN 6,694,398 to Zhao et al teaches recognizing and handling fast and regular interrupts differently.

PN 5,386,563 to Thomas, deceased teaches recognizing and handling fast and slow exceptions including the use of shadow registers for the program counter and PSW for the fast exceptions.

PN 5,701,493 to Jaggar teaches recognizing and handling fast and slow exceptions including the use of shadow registers for the program counter and PSW for the fast exceptions.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 703 305 9656. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703 305 4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PRM
September 21, 2004

PAUL R. MYERS
PRIMARY EXAMINER